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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,166	09/24/2003	Toshio Kimura	1035-473	4031
23117 7590 01/22/2009 NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203				
EXAMINER				
ARENA, ANDREW OWENS				
ART UNIT		PAPER NUMBER		
2811				
MAIL DATE		DELIVERY MODE		
01/22/2009		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/668,166

Applicant(s)

KIMURA ET AL.

Examiner

Andrew O. Arena

Art Unit

2811

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 November 2007 and 02 July 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2, 4, 5, 7-9, 11-13, 15-17, 19 and 20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4, 5, 7-9, 11-13, 15-17, 19 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-949)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

In view of the Appeal Brief filed on 08/27/2008, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Lynne A. Gurley/

Supervisory Patent Examiner, Art Unit 2811.

Comment on reopening prosecution

Upon reconsidering the claims for appeal, it became clear that the amendment filed 11/01/2007 necessitated new grounds of rejection under 35 U.S.C. § 112 which was not presented in the final rejection dated 1/28/2008. Additionally, **the finality of that action is withdrawn.**

It is essential to the appeal that the scope of the claims be definite.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 4, 5, 7, 9, 11, 13, 15, 17 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 7 recite “said least one through electrode” which is not only grammatically incorrect, but creates confusion as to which of the previously recited through electrodes is being referenced. Dependent claims inherit this indefiniteness.

It seems that claims 1 and 7 intend to require a limitation similar to that recited in the last three lines of claim 8, which does not suffer from the above-cited indefiniteness.

Claim Rejections - 35 USC § 103

Claims 1, 2, 4, 5, 7, 8, 9, 11, 12, 13, 15, 16, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as obvious over Sumikawa in view of Anderson (both already of record).

RE claim 1, Sumikawa discloses (Figs 3, 6, 7; col 5 ln 20-41) a semiconductor device comprising (referring to Fig 3):

a plurality of spaced apart through electrodes (2; col 3 ln 32) with equal cross sectional areas in a semiconductor chip (1; col 3 ln 30) which through electrodes electrically link a front surface of the chip to a back surface of the chip (col 3 ln 38-40), wherein

a least one of the plurality of through electrodes is in communication with a power supply (inherent; this must be true in order to operate the chip),

at least another one of the plurality of through electrodes is in communication with ground (inherent; this must be true in order to operate the chip),

at particular signal-routing through electrode is formed of only one of the plurality of through electrodes (e.g., 22a in Fig 4; col 4 ln 53); and

at least one of the plurality of through electrodes is a non-contact through electrode (22b) which is electrically isolated from the chip (col 4 ln 3-6; col 4 ln 45-55) so that said at least one through electrode is not electrically connected to any electrode pad of the chip (22b is not connected to any of 23a, 23b, 24a or 24b).

Sumikawa differs from the claimed invention only in not disclosing a plurality of through electrodes connected to one another to form a high-current through electrode.

Anderson discloses an analogous stacked-chip semiconductor device (col 3 ln 5; Fig 3) comprising (Fig 2) a plurality of spaced apart electrodes (205) on a semiconductor chip (200) wherein at least two electrodes are connected to one another to form a first high-current electrode (210) for power supply (VDD; col 4 ln 8-12), at least another electrodes are connected to one

another to form a second high-current electrode (220) for ground supply (GND; col 4 ln 3-7), and a particular signal-routing electrode (205) is formed of only one electrode.

It is fundamental in electrical arts that resistance is proportional to area; one of ordinary skill instantly appreciates that connecting a plurality of electrodes increases the effective cross-sectional area of the conductor and carries a given signal with less loss.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Anderson, at least two of the plurality of through electrodes are connected to one another to form a first high-current through electrode that is in communication with a power supply and at least another two of the plurality of through electrodes are connected to one another to form a second high-current through electrode that is in communication with ground; at least to reduce power losses.

RE claim 2, Sumikawa discloses at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip (col 4 ln 53-55).

RE claim 4, the combined device discloses both of the first number and the second number is two or greater (Anderson: Fig 2), so that each of the first (210) and second (220) high-current through electrodes is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas the signal-routing electrode (205) is made up of only one of the through electrodes.

RE claim 5, Sumikawa discloses multiple stacked semiconductor chips, each of the semiconductor chips including a semiconductor device according to claim 1.

RE claim 7, Sumikawa discloses (Figs 3, 4, 6, 7; col 5 ln 20-41) a chip-stack semiconductor device comprising:

a plurality (Fig 4) of stacked semiconductor chips (1, 21; col 4 ln 21-22), each of the semiconductor chips including a plurality of through electrodes (2, 22; col 4 ln 36) with equal cross-sectional areas therein linking a front surface to a back surface thereof,

wherein at least one first high-current electrode is connected to a power supply and at least one second high-current electrode is connected to ground (inherent; this must be true in order to operate the chip), and a signal-routing electrode connecting a front [surface to] a back surface of one of the semiconductor chips is made up of only one of the through electrodes (e.g., 22a in Fig 4; col 4 ln 53), and

at least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated from the chip (col 4 ln 3-6; col 4 ln 45-55) so that said at least one through electrode is not electrically connected to any electrode pad of the chip (22b is not connected to any of 23a, 23b, 24a or 24b).

Sumikawa differs from the claimed invention only in not disclosing a plurality of through electrodes connected to one another to form a high-current through electrode.

Anderson discloses an analogous stacked-chip semiconductor device (col 3 ln 5; Fig 3) comprising (Fig 2) a plurality of spaced apart electrodes (205) on a semiconductor chip (200) wherein at least two electrodes are connected to one another to form a first high-current electrode (210) for power supply (VDD; col 4 ln 8-12), at least another electrodes are connected to one another to form a second high-current electrode (220) for ground supply (GND; col 4 ln 3-7), and a particular signal-routing electrode (205) is formed of only one electrode.

It is fundamental in electrical arts that resistance is proportional to area; one of ordinary skill instantly appreciates that connecting a plurality of electrodes increases the effective cross-sectional area of the conductor and carries a given signal with less loss.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Anderson, at least one of a first high-current through electrode connected to a power supply and a second high-current through electrode connected to ground is made up of at least two of the through electrodes which are electrically connected to one another; at least to reduce power losses.

RE claim 8, Sumikawa discloses (Figs 3, 4, 6, 7; col 5 ln 20-41) a chip-stack semiconductor device comprising:

multiple stacked (Fig 4) semiconductor chips (1, 21; col 4 ln 21-22), each of the semiconductor chips including a number of through electrodes (2, 22; col 4 ln 36) with equal cross-sectional areas therein linking a front surface to a back surface thereof, the number of the through electrodes being determined (no implied structure: MPEP 2114) in accordance with a magnitude of an electric current to be conducted therethrough, wherein

a number of through electrodes are connected to [a] either a ground terminal or a power supply terminal of that semiconductor chip (inherent; this must be true in order to operate the chip) and a number of through electrodes are connected to a particular signal terminal (e.g., 22a in Fig 4; col 4 ln 53), and

at least one of the through electrodes is a non-contact through electrode which is not electrically connected to any electrode pad of the chip in which it is formed (22b is not connected to any of 23a, 23b, 24a or 24b; col 4 ln 3-6; col 4 ln 45-55).

Sumikawa differs from the claimed invention only in not disclosing a plurality of through electrodes connected to one another to form a high-current through electrode.

Anderson discloses an analogous stacked-chip semiconductor device (col 3 ln 5; Fig 3) comprising (Fig 2) a plurality of spaced apart electrodes (205) on a semiconductor chip (200) wherein at least two electrodes are connected to one another to form a first high-current electrode (210) for power supply (VDD; col 4 ln 8-12), at least another electrodes are connected to one another to form a second high-current electrode (220) for ground supply (GND; col 4 ln 3-7), and a particular signal-routing electrode (205) is formed of only one electrode.

It is fundamental in electrical arts that resistance is proportional to area; one of ordinary skill instantly appreciates that connecting a plurality of electrodes increases the effective cross-sectional area of the conductor and carries a given signal with less loss.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Anderson, at least one of a first high-current through electrode connected to a power supply and a second high-current through electrode connected to ground is made up of at least two of the through electrodes which are electrically connected to one another; at least to reduce power losses.

RE claims 9, 11, & 12, the combined device discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent; e.g., Sumikawa Fig 4).

Sumikawa as modified above differs from the claimed invention only in not expressly disclosing the number of through electrodes used in connecting different numbers of chips.

It is well known that a larger total conductor cross-section is used for a longer conduction path length to reduce impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that a number of those through electrodes which connect $n+1$ or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2; at least to reduce impedance.

RE claims 13, 15, & 16, the combined device discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent; e.g., Sumikawa Fig 4).

Sumikawa as modified above differs from the claimed invention only in not expressly disclosing the number of through electrodes is increased with interconnect line length.

It is well known that a larger total conductor cross-section is used for a longer conduction path length to reduce impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that as an interconnect line length through the multiple stacked semiconductor chips is longer, more through electrodes are provided for the first high-current through electrode and the second high-current through electrode; at least to reduce impedance.

Furthermore, the recitation “as [a length]...is longer, more through electrodes” is not a structural limitation but seems to be either a recitation of indented use and does not impart patentability to apparatus claims such as these. See MPEP § 2114.

RE claims 17, 19, & 20, the combined device discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent).

Sumikawa as modified above differs from the claimed invention only in not expressly disclosing numbers of through electrodes are increased in proportion to an interconnect line length.

It is well known that a larger total conductor cross-section is used for a proportionally longer conduction path length to reduce impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that numbers of the first and second high-current through electrodes are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips; at least to reduce impedance.

Furthermore, the recitation "are increased in..." is not a structural limitation but seems to be either a recitation of indented use or manner of operating; such recitations do not impart patentability to apparatus claims such as these. See MPEP § 2114.

Response to Arguments

The arguments filed 11/01/2007 were fully considered but are not persuasive.

The argument that "Sumikawa makes very clear that both penetrating electrodes are electrically connected to wiring patterns of the chip" (reply pg 9 ln 5) stand in stark contrast to Figure 4 of Sumikawa, which shows both electrodes (2a, 22) in contact with pads (4a, 3a, 23a) and electrodes (2b, 22b) not in contact with any pads.

The allegation of impermissible hindsight (reply pg 9, last paragraph) is not convincing. A person of ordinary skill in any electrical art, of necessity, understands that $\text{resistance} = \text{constant} * \text{length} / \text{X-sec area}$. See MPEP § 2141.03 citing to Hiyamizu.

The argument that one "would apply...Anderson" (reply pg 10 ln 3-5) attempts to limit the rationale, but one may use their knowledge. See MPEP § 2144(I).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. For more info about PAIR, see <http://pair-direct.uspto.gov>. For questions PAIR access, contact the Electronic Business Center at 866-217-9197 (toll-free). For assistance from a USPTO Customer Service Rep or access to the automated info system, call 800-786-9199 or 571-272-1000.

/Andrew O. Arena/
Examiner, Art Unit 2811
13 January 2009

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit
2811